Future Perspective of Non-Volatile Memory

Stefan Lai, PhD, Fellow IEEE

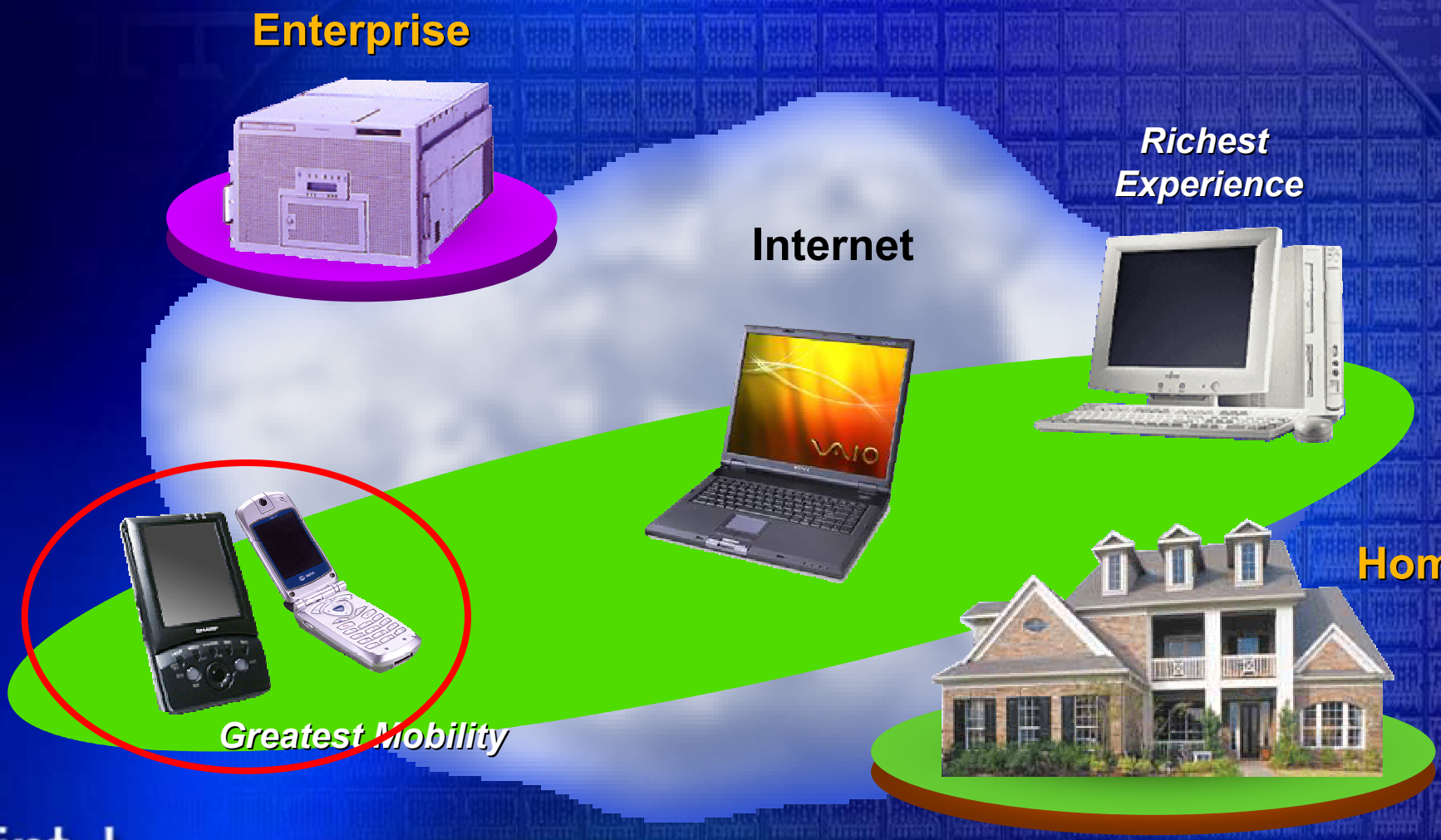
Intel Corporation

Vice President, Technology and Manufacturing Group

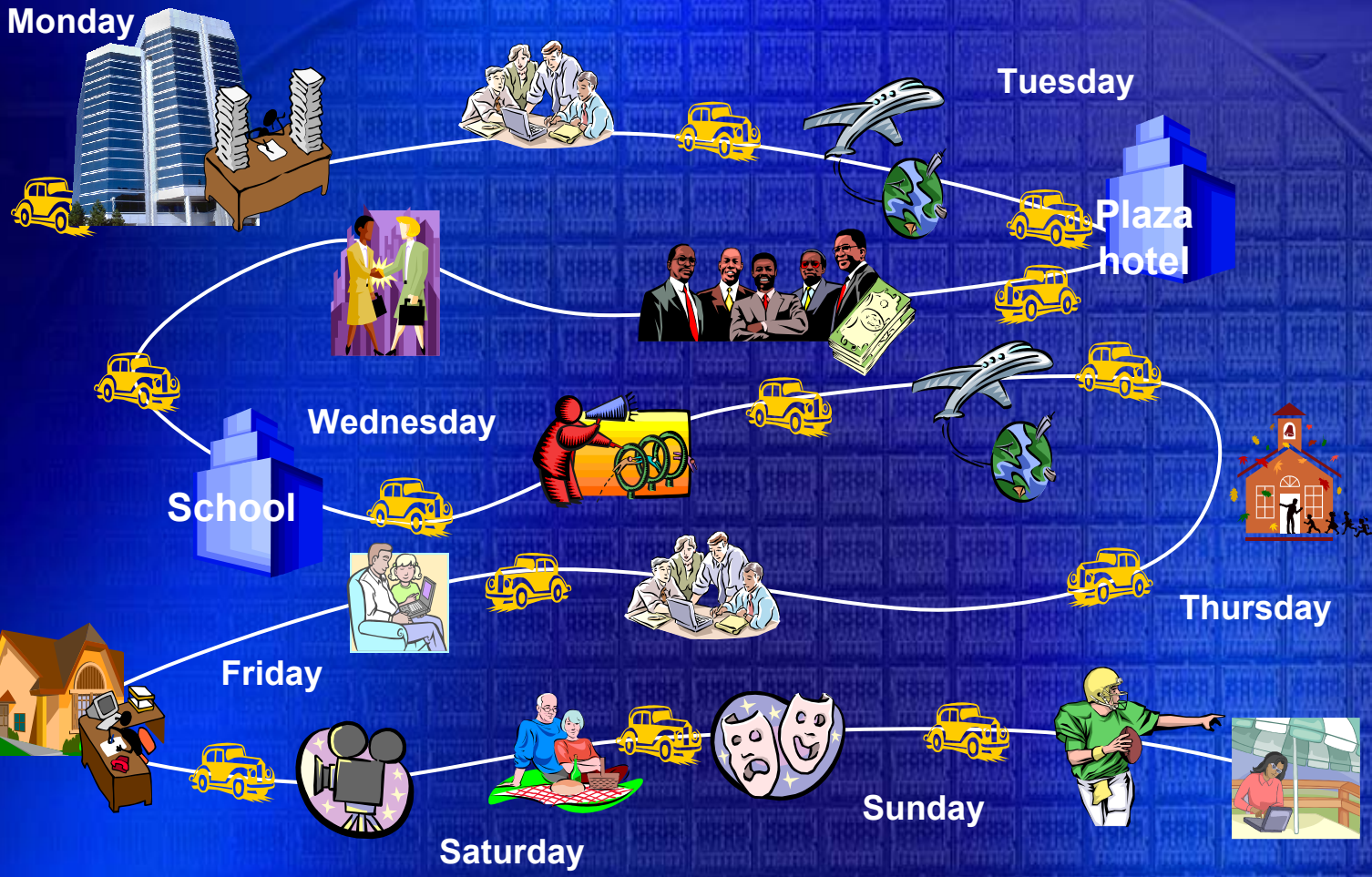
Director, California Technology and Manufacturing

Why Non-Volatile Memories?

Mobile Lifestyle: Data Anytime, Anywhere



Computing is Going Mobile



Mobility is Inevitably Becoming our Work Style & Lifestyle

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Memories for Mobility

- Non-volatile = low power: power down to save power
- Low cost: one memory for program and data storage
- ≠ magnetic hard disk: need solid state, low power, rugged
- Small form factor and light weight

Moore's Law in NV Memory

- Moore's Law will continue through innovation
  - Process complexity will increase to address fundamental limits of physics
- To maintain Moore's Law cost learning curve, difficult to do it by transistor technology alone
  - New opportunity for new memory structures and new materials
- Current mainstream NV memory technologies of ETOX and NAND will continue to be the key technologies for more than 5 years out
- Intense research activities to identify scalable memory technologies for 5 year and beyond

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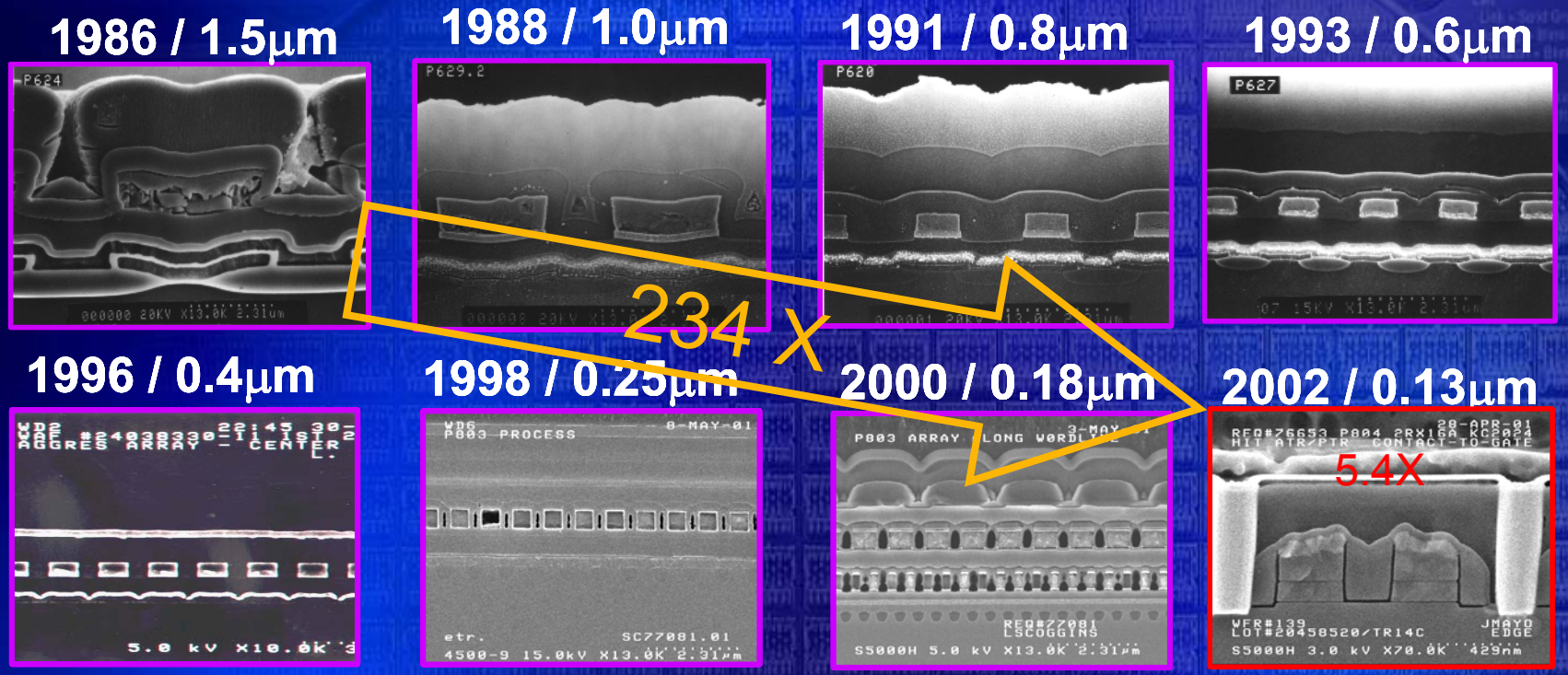
Moore's Law will Continue with ETOX® Flash

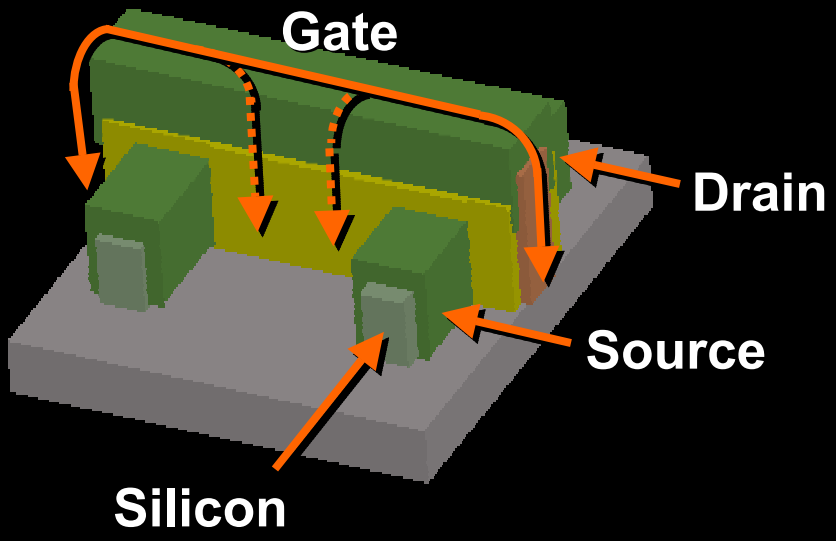
- Currently shipping 8th generation of ETOX® flash memory in high volume
  - ~50% cell size reduction per generation
- Good visibility into 90 nm and 65 nm generation
- Current projection shows scaling continues at 45 nm node but challenged to meet 50% goal
- Further innovation required to maintain cost learning curve
- Industry trend: complex transistor structure to meet scaling challenges

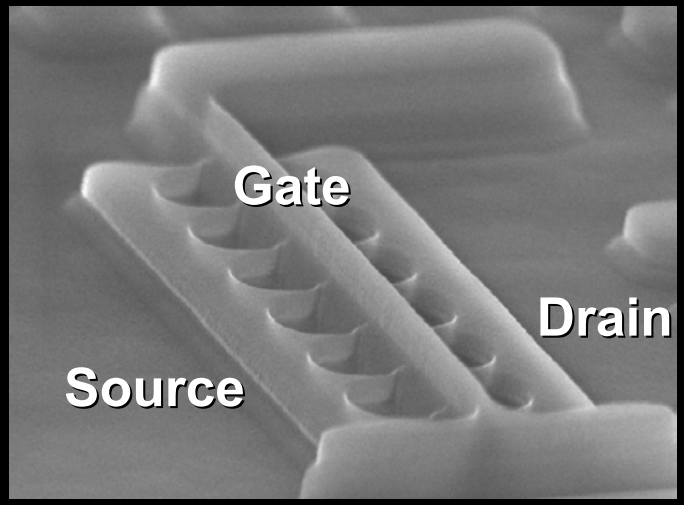
ETOX® Technology Scaling



- 18 years and 8 Generations of ETOX® to 0.13 µm

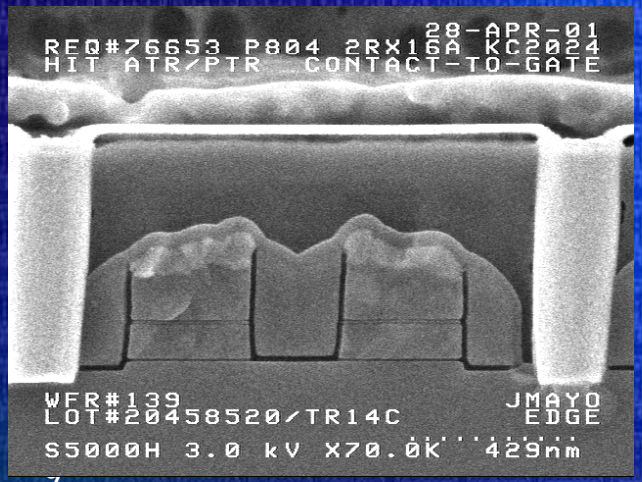
Example of Future Transistor





Source: Intel

Example of Current Flash Memory Cell



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New Materials in Silicon Technology

- The semiconductor industry has been addressing the performance and cost issues by introducing new materials
  - Tantalum pentoxide for DRAM storage dielectric
  - Cobalt and Nickel for S/D formation
  - Copper and low k dielectric for interconnect
  - High K dielectric for transistor gate
- For non-volatile memories, new memory materials provide new opportunities for further memory cost reduction

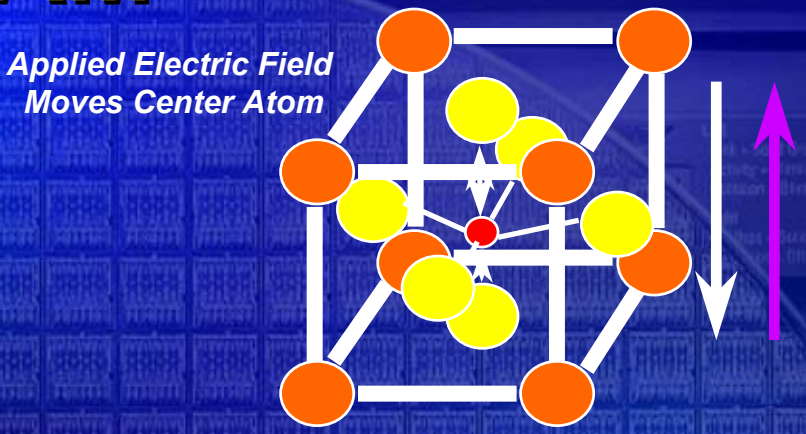
Review of New Memories

- Explosion of research and development on new memory technology and material
- Scopes range from full scale manufacturing development to industrial labs to new startup companies to university research
- Time frames range from product now to nano technology research 10-20 years out
- No perfect memory, each has its own unique challenge

Examples of new memory technologies

FeRAM

- Operation
  - Selected PZT crystalline materials have bi-stable center atom
  - Data is stored by applying an voltage to polarize the internal dipoles “Up” or “Down”
  - Reading by sensing the displacement current
  - Fast read/write < 100 nSec
  - Destructive read, limited number of read cycles due to fatigue
  - Very low power consumption

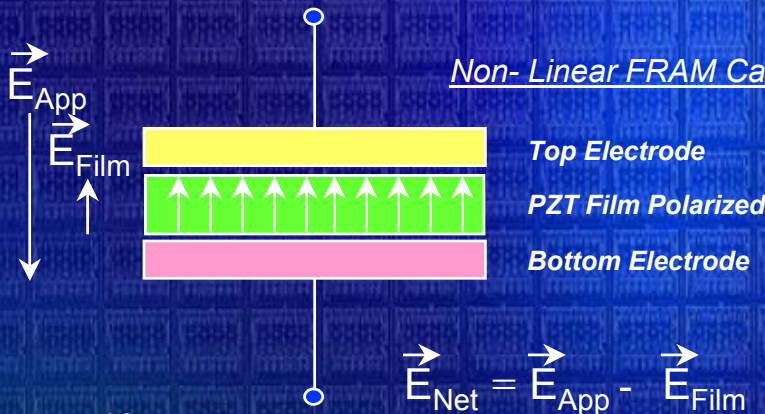


Perovskite Crystal Unit Cell
PZT (PbO, ZrO_2, TiO_2) Lead-Zirconate-Titanate

Tetra/Pentavalent Atom

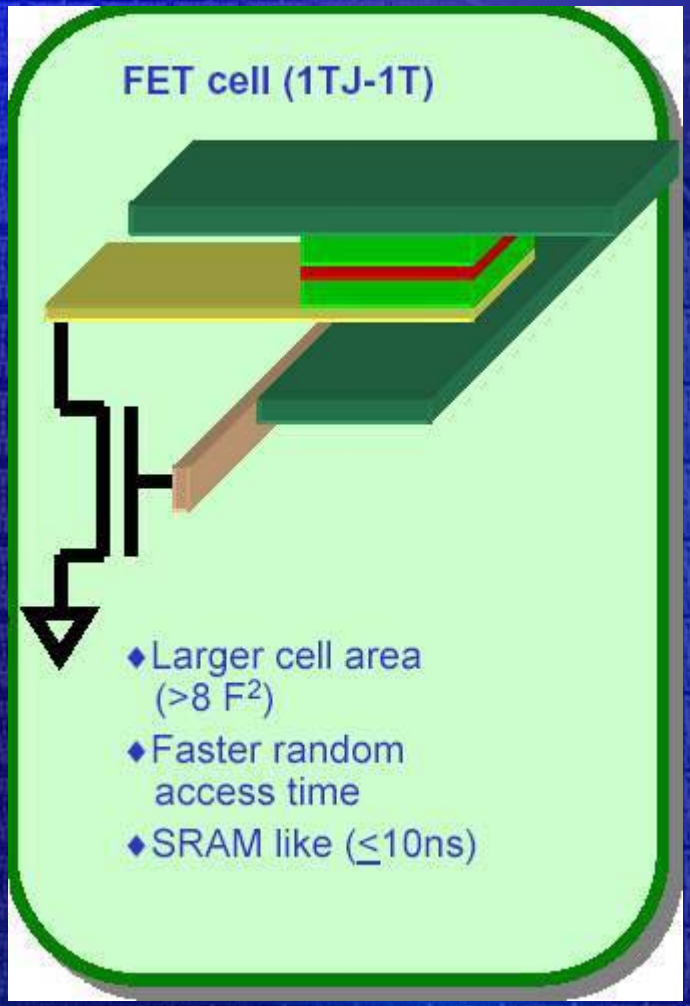
Di/Monovalent Metal Atoms

Oxygen Atoms



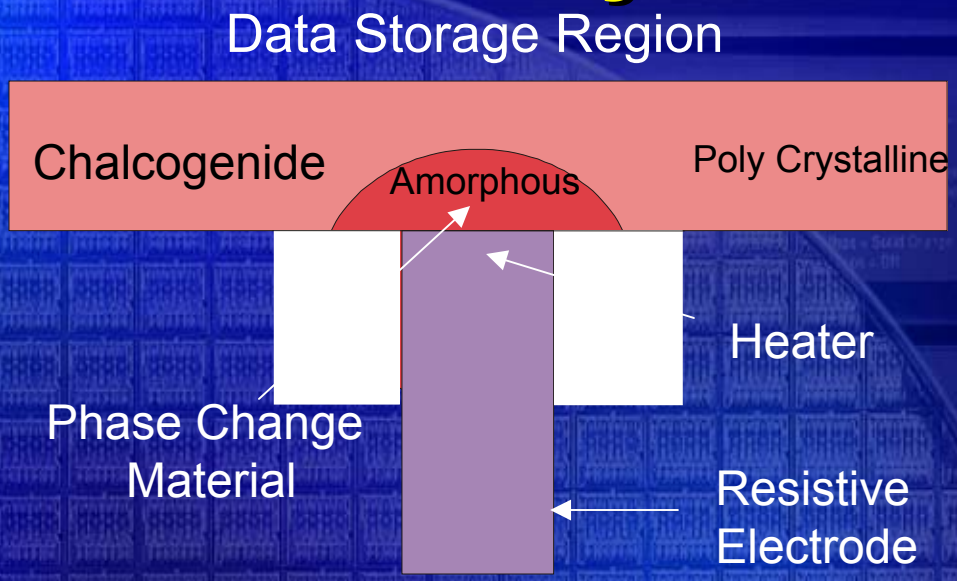
MRAM

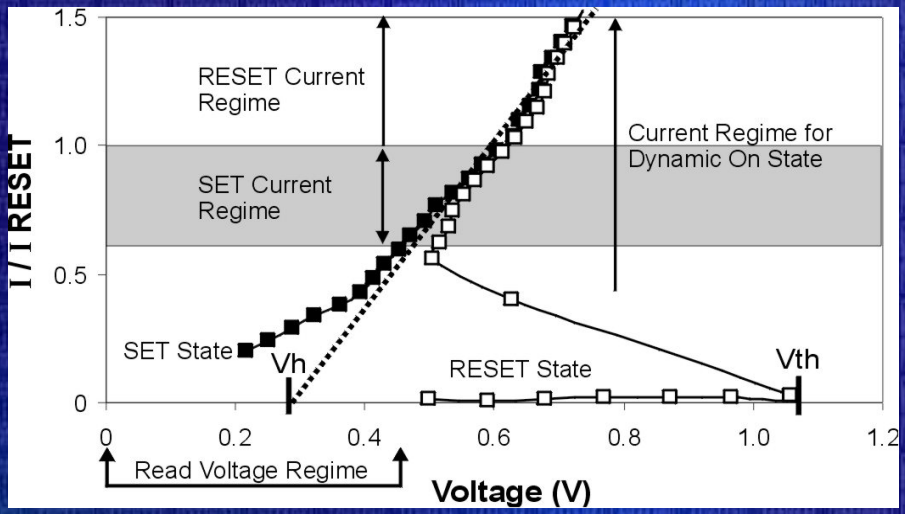
- Operation
  - Cell is 1 MJT + 1 Transistor
  - Electric current switches the magnetic polarity of sense layer
  - Change in magnetic polarity sensed as resistance change in tunnel junction
  - Non destructive read
  - Very fast read/write performance, < 10 nSec reported
  - Unlimited number of R/W endurance
  - Relatively high write current



Ovonics Unified Memory

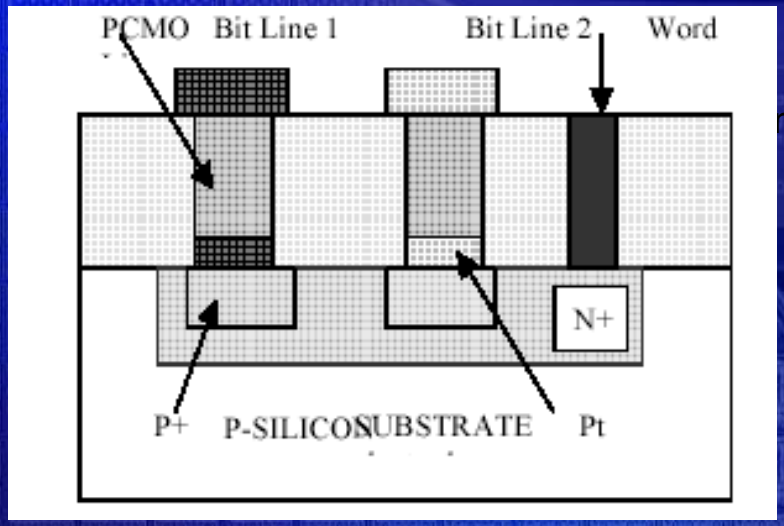
- Operation
  - Chalcogenide material alloys used in re-writable CDs and DVDs
  - Electrical energy (heat) converts the material between crystalline (conductive) and amorphous (resistive) phases
  - Cell reads by measuring resistance
  - Non-destructive read
  - ~10^{12} write/erase cycles
  - Medium write power
  - Relatively easy integration with CMOS





Complex Metal Oxide RRAM

- Operation
  - PCMO material, Complex metal oxide studied for high temp superconductivity
  - Change in resistance with applied electric field
  - Low resistance with forward bias, high resistance when reverse electric field applied
  - Low field read by measuring resistance
  - Relatively low power write



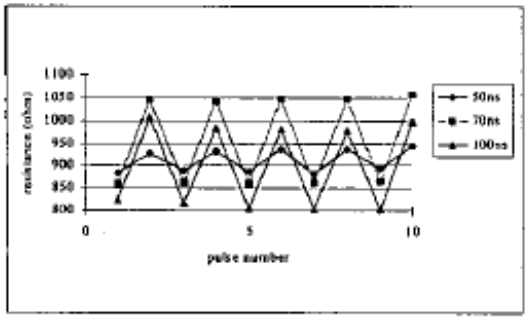
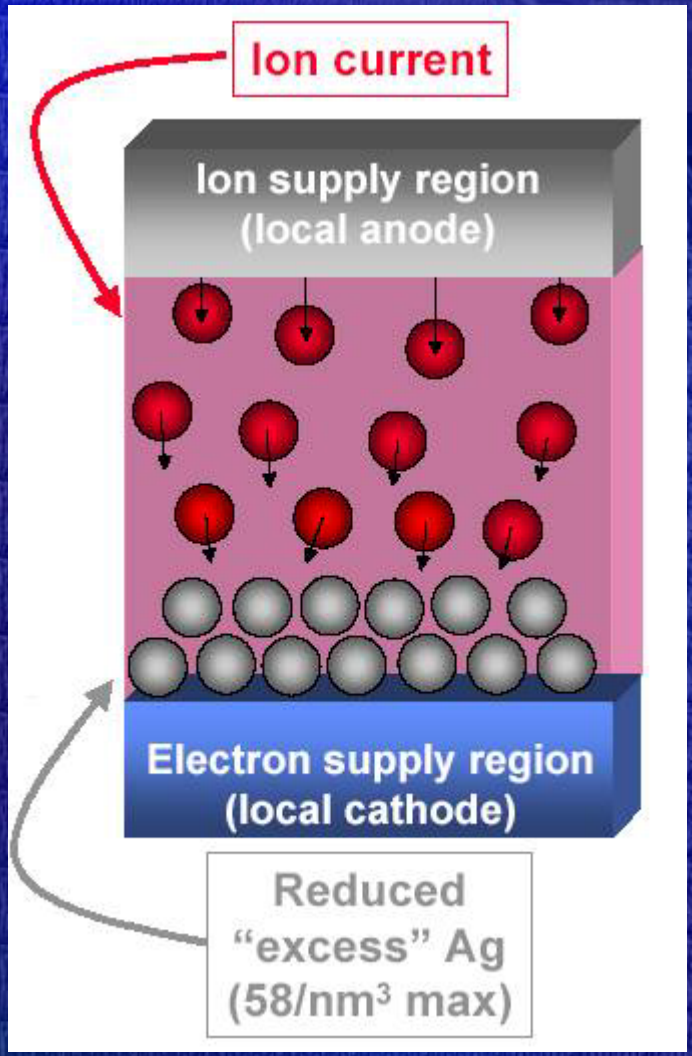


Fig.8 Positive pulse writes the resistor to high resistance-state. Negative pulse reset the resistor to low resistance-state. Programming efficiency depends strongly on pulse width

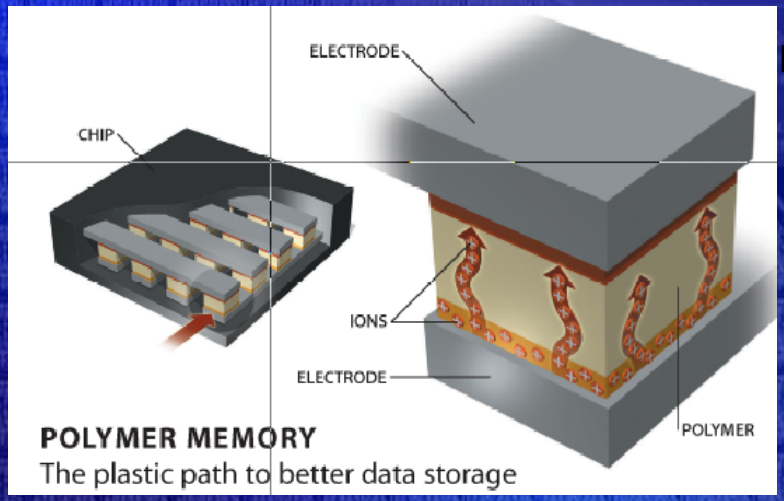
Programmable Metallization Cell

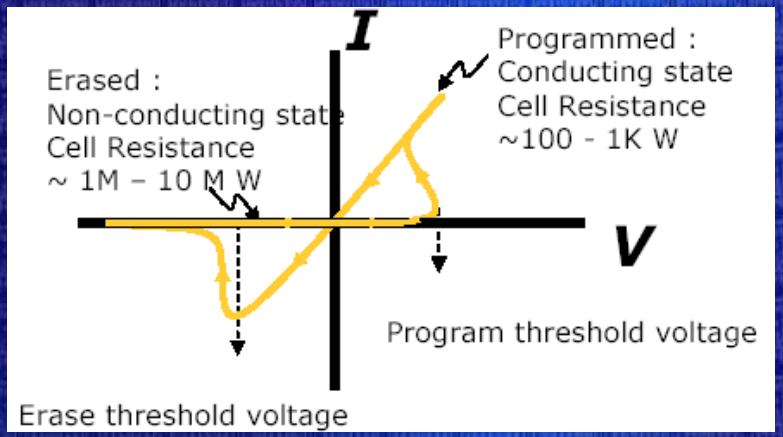
- Operation
  - Silver “dissolved” in chalcogenide
  - Change in resistance with applied electric field driving silver to form low resistance path
  - Reversible with reverse field
  - Low field read with no disturb
  - Very fast write and relatively low power



Resistance Polymer Memory

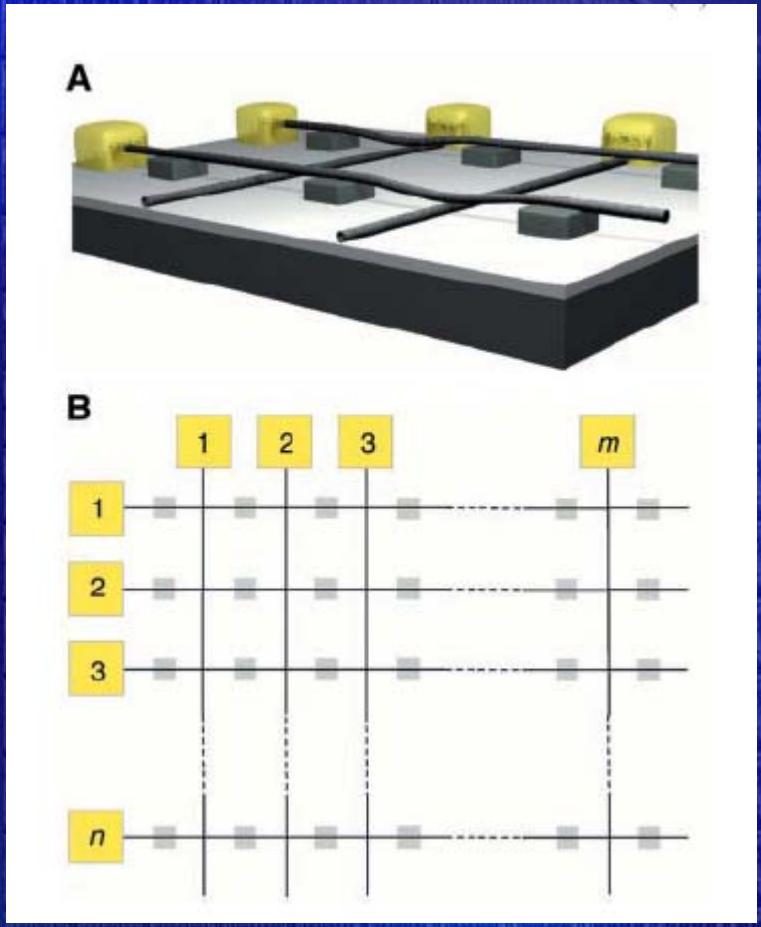
- Operation
  - Polymer material with special formulation
  - Change in resistance due to ionic transport with applied electric field
  - Low resistance when ionic conductance paths formed, high resistance when process is reversed when paths broken
  - Low field read with no read disturb
  - Low cost with polymer





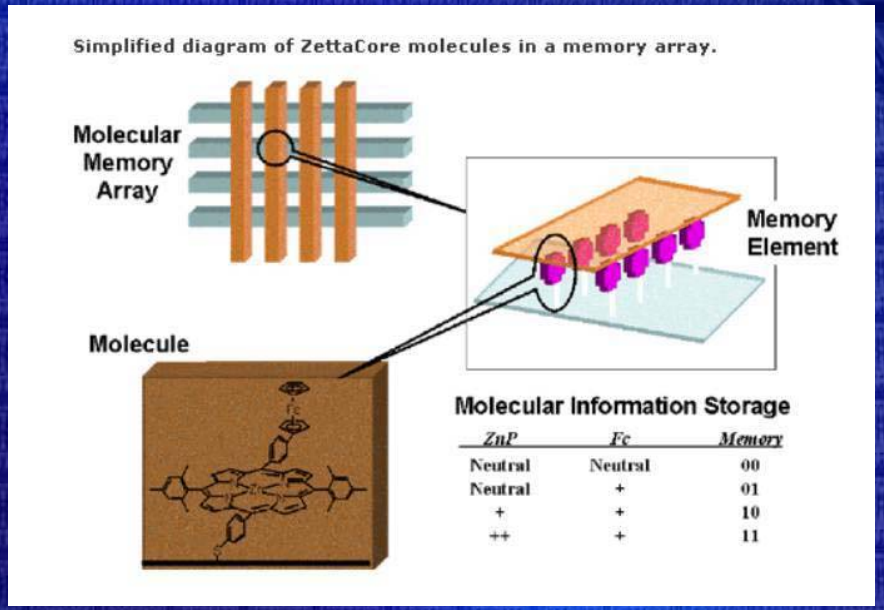
Carbon Nanotube Switches

- Operation
  - Carbon nanotube suspended in crossbar architecture
  - Electrostatic field attracts the nanotube and held together by van der Waals force
  - Reverse bias repulse the wires
  - Reading by low vs high resistance
  - Array Architecture TBD



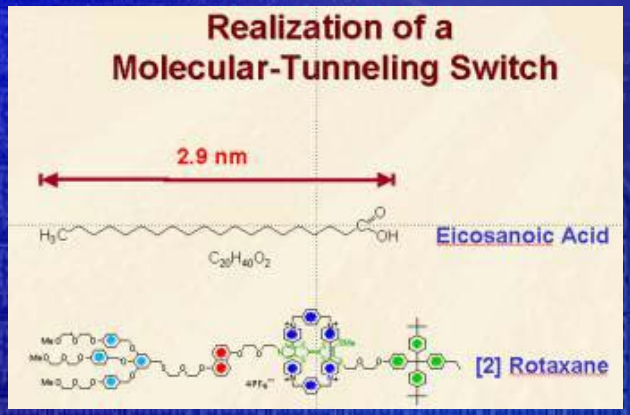
Molecular Memory

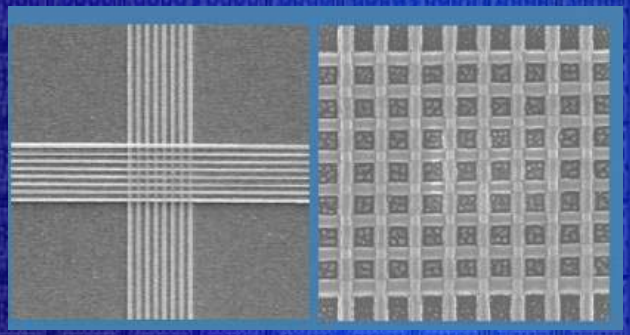
- Operation
  - Molecules in cross point array
  - Change in electronic states in Redox process with applied voltage
  - Memory state sensed by charge displacement
  - More than 1 state can be stored by design of molecule (up to 8 demonstrated)

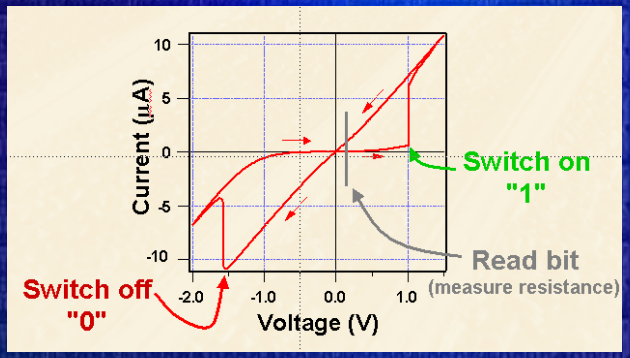


Molecular Tunnel Memory

- Operation
  - Molecules in cross point array
  - Change in resistance with applied electric field
  - Memory state sensed by measured resistance change

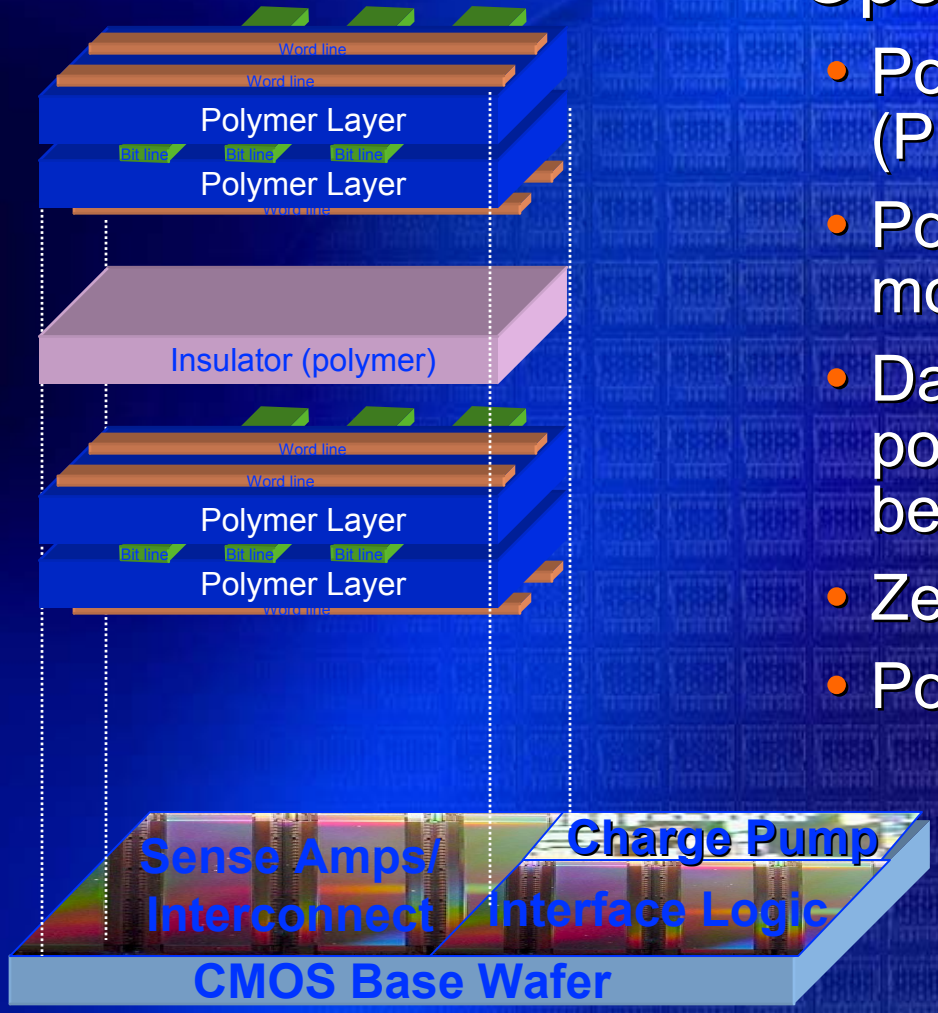


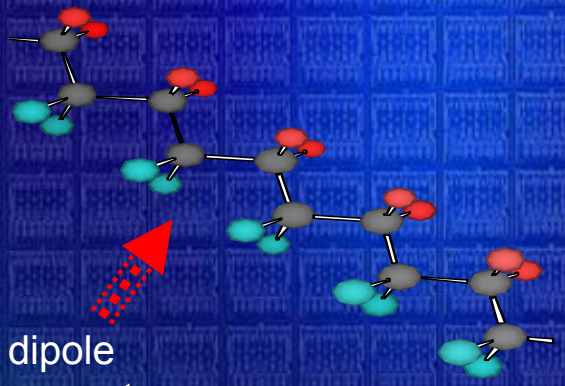




Ferroelectric Polymer Memory

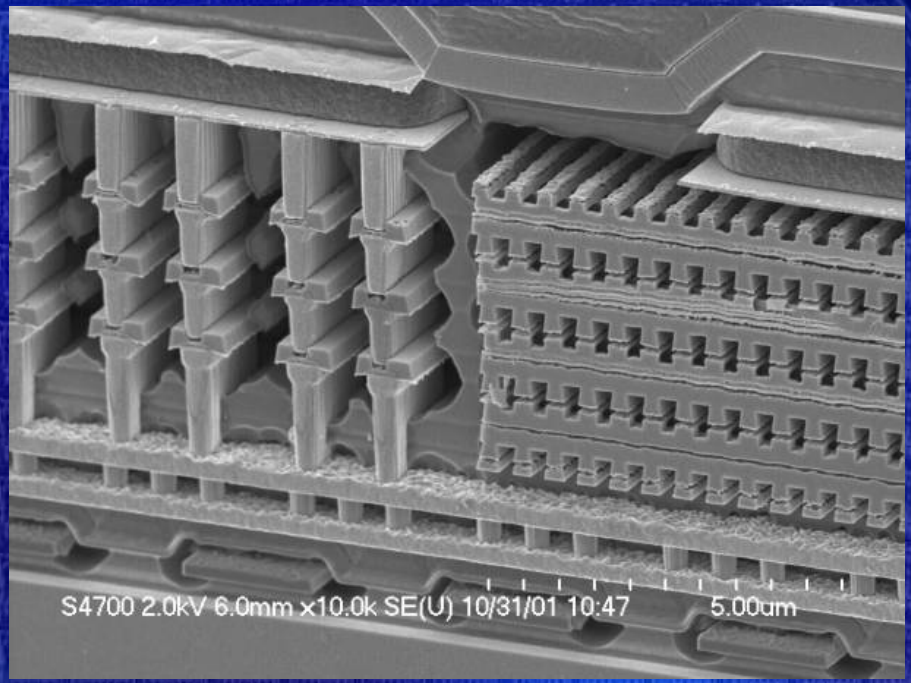
- Operation
  - Polymeric Ferroelectric RAM (PFRAM)
  - Polymer chains with a dipole moment
  - Data stored by changing the polarization of the polymer between metal lines
  - Zero transistors per bit of storage
  - Polymer layers can be stacked





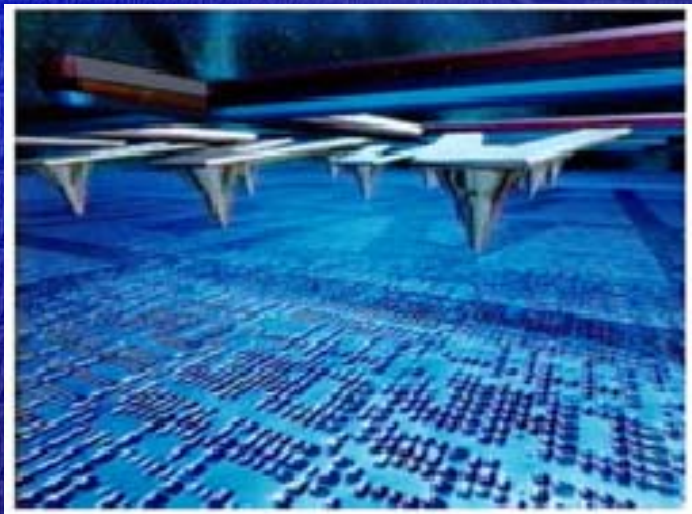
3D One Time Program Memory

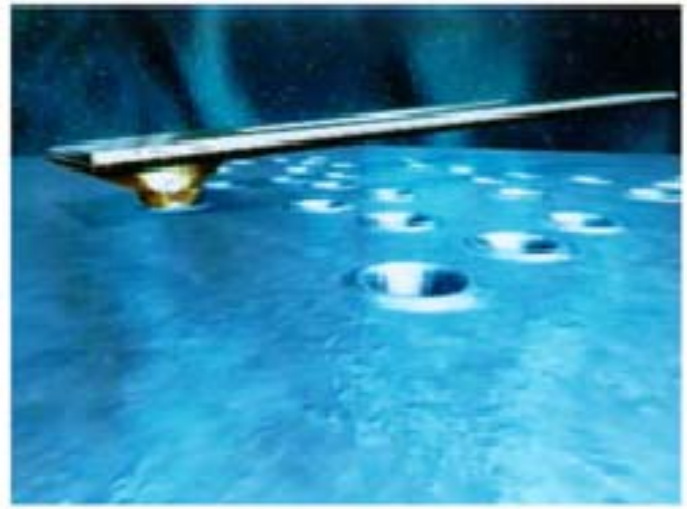
- Operation
  - Multi-layer one time programmable diodes at minimum lithography dimensions
  - Simplified architecture with minimum number of metal lines
  - Zero transistor per cell
  - Standard CMOS transistors under and outside array, process cost amortized over multiple memory cells
  - Significant lower cost compared to single layer



Millipede Memory

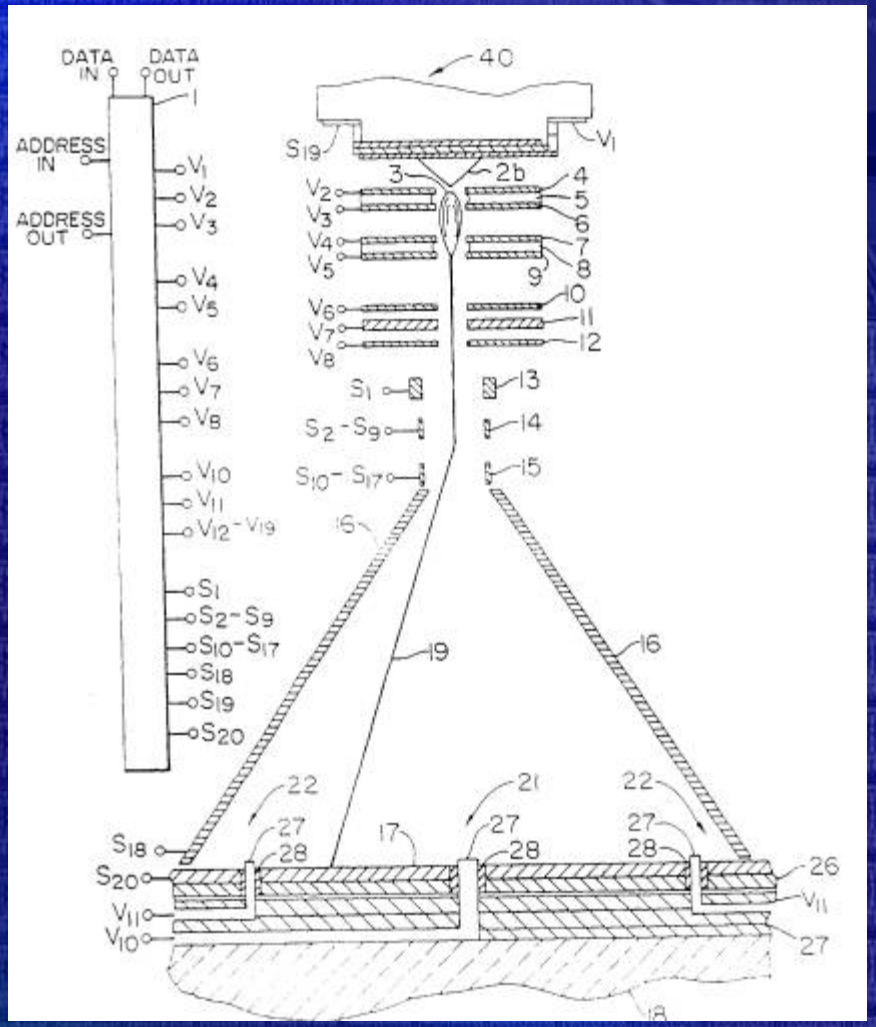
- Operation
  - Basic concept similar to punch cards
  - Thermally assisted, rewritable displacement media, PMMA
  - Large array of independently Z-axis controlled tips
  - Low moving mass
  - Direct point to point motion, no rotational latency
  - Low power, no motors, actuators
  - High data transfer rates, concurrent data transfer to/from multiple tips
  - Packaging similar to hermetic devices





Spin Polarized E Beam Magnetic Memory

- Operation
  - Basic concept similar to Magnetic Hard Drive
    - Mechanical arm -> spin polarized E Beam
    - Spinning Magnetic Media -> steered E Beam
  - Much lower first read latency, first access limited by E Beam steering; fast read with E Beam
  - Lower power, no motor, no arm actuator
  - No moving part, rugged, vacuum space required
  - Not as small or compact as all solid state memories



A Simplified View

- All above memories can be divided into two broad categories:

1. X-Y addressable, limited by lithography and follows Moore's Law
2. Seek and scan memory, no lithography, limited by scan mechanism, size and density of storage areas in storage medium

Breaking the scaling barrier

- Memory technologies requiring transistor switch will be limited in scaling -> FeRAM, MRAM, diode switch scales better -> OUM, RRAM

➔ Follows Moore's Law limited by transistor/diode

- Simple cross point switch with no transistor or diode more scalable: molecular memories

➔ Continue Moore's Law beyond transistor age

- Multi-layer memories have the potential to be lowest cost for litho defined memory

➔ Drop below historical Moore's Law

- Seek and scan can be the lowest cost but involves new memory storage and sense mechanism

➔ May go faster then Moore's Law (e.g. HDD)

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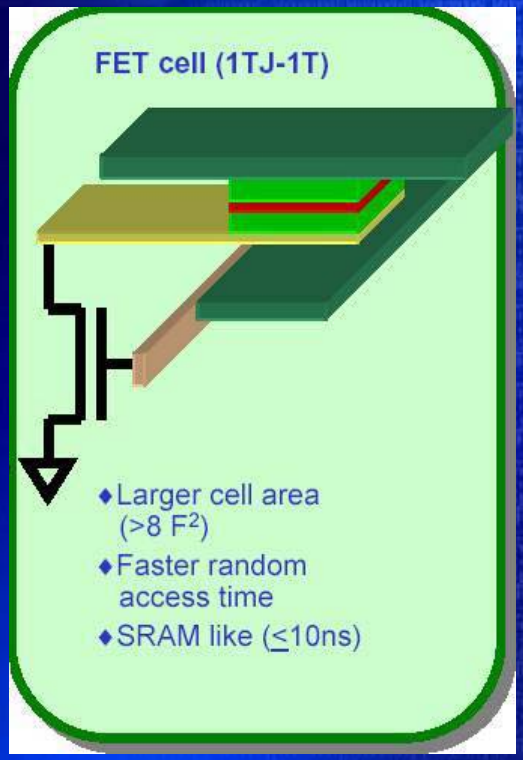
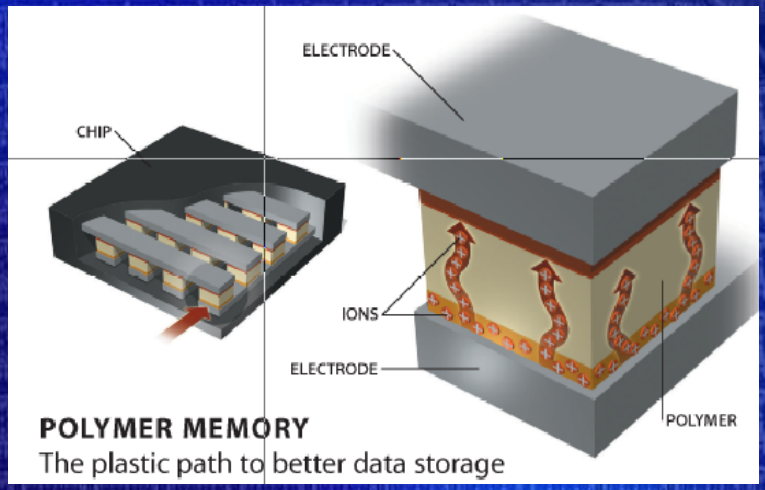
No transistor switch better than transistor switch

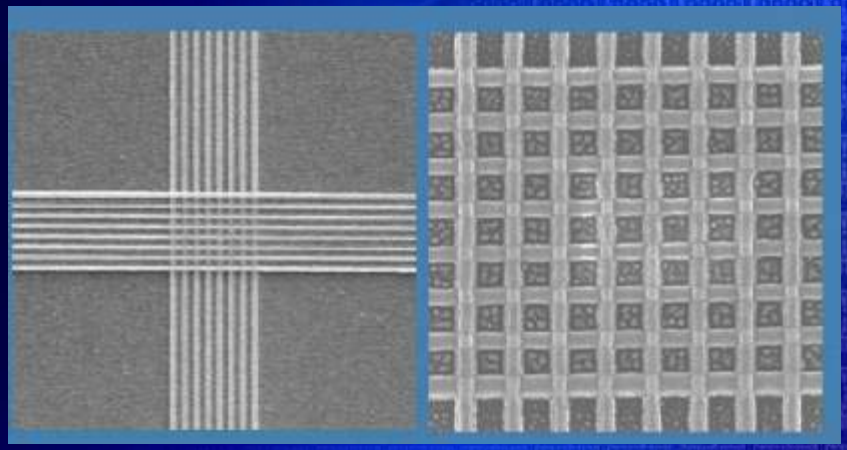


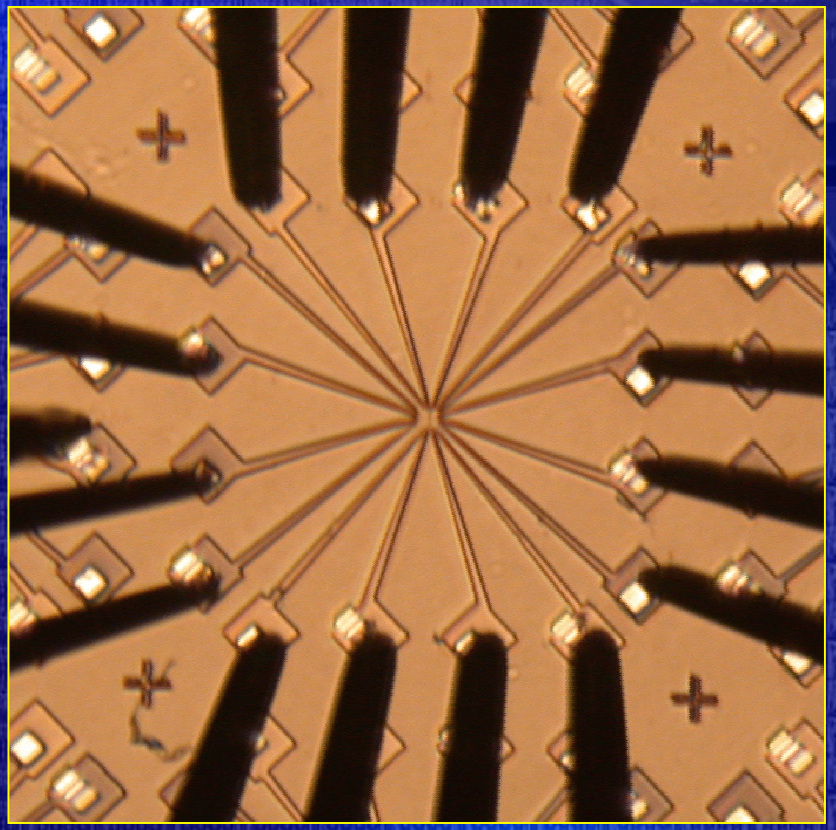
Big



Small

Small is not that small





- X-Y addressable memory is always limited by the limiting lithography steps: have to connect to the real world circuits
- Either self assembled circuits at the smaller geometry or new innovative architecture

Breaking the scaling barrier

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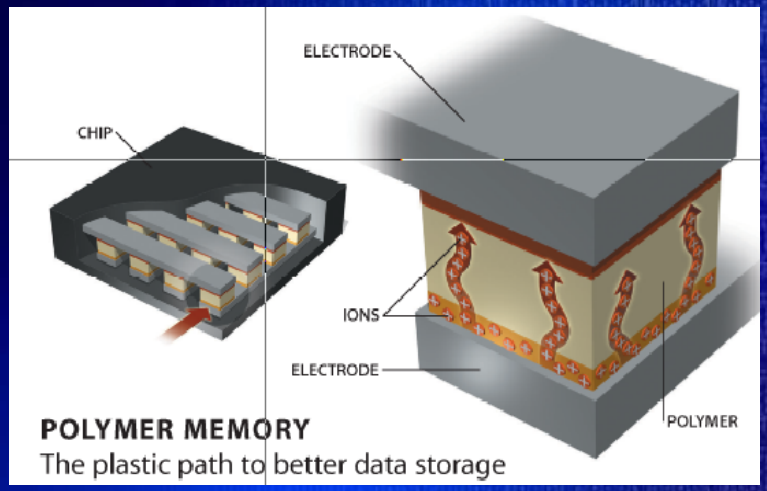
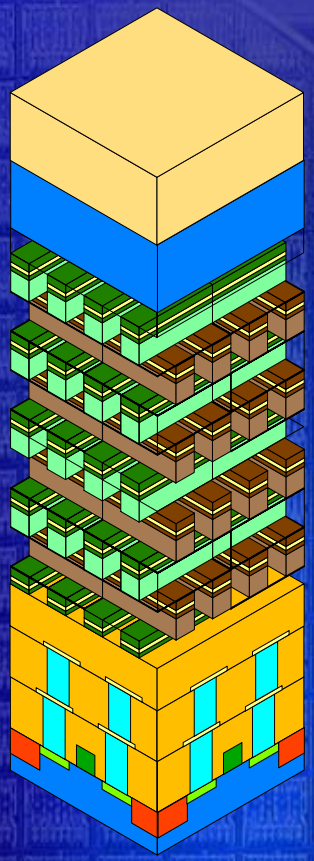
➔ May go faster then Moore's Law (e.g. HDD)

Multi-layer is smaller





Single Layer cell area = $4\ \lambda^2$

Multi Layer cell area = $4\ \lambda^2$/ N (number of layers)

Breaking the scaling barrier

- Memory technologies requiring transistor switch will be limited in scaling -> FeRAM, MRAM, diode switch scales better -> OUM, RRAM

➔ Follows Moore's Law limited by transistor/diode

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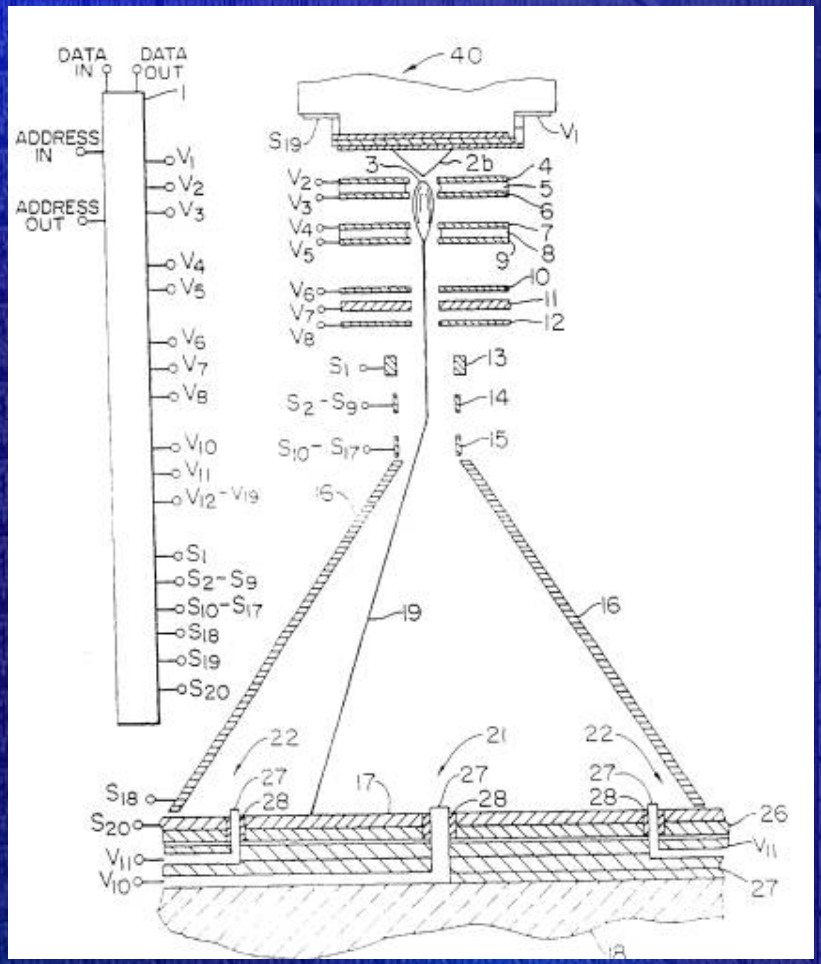
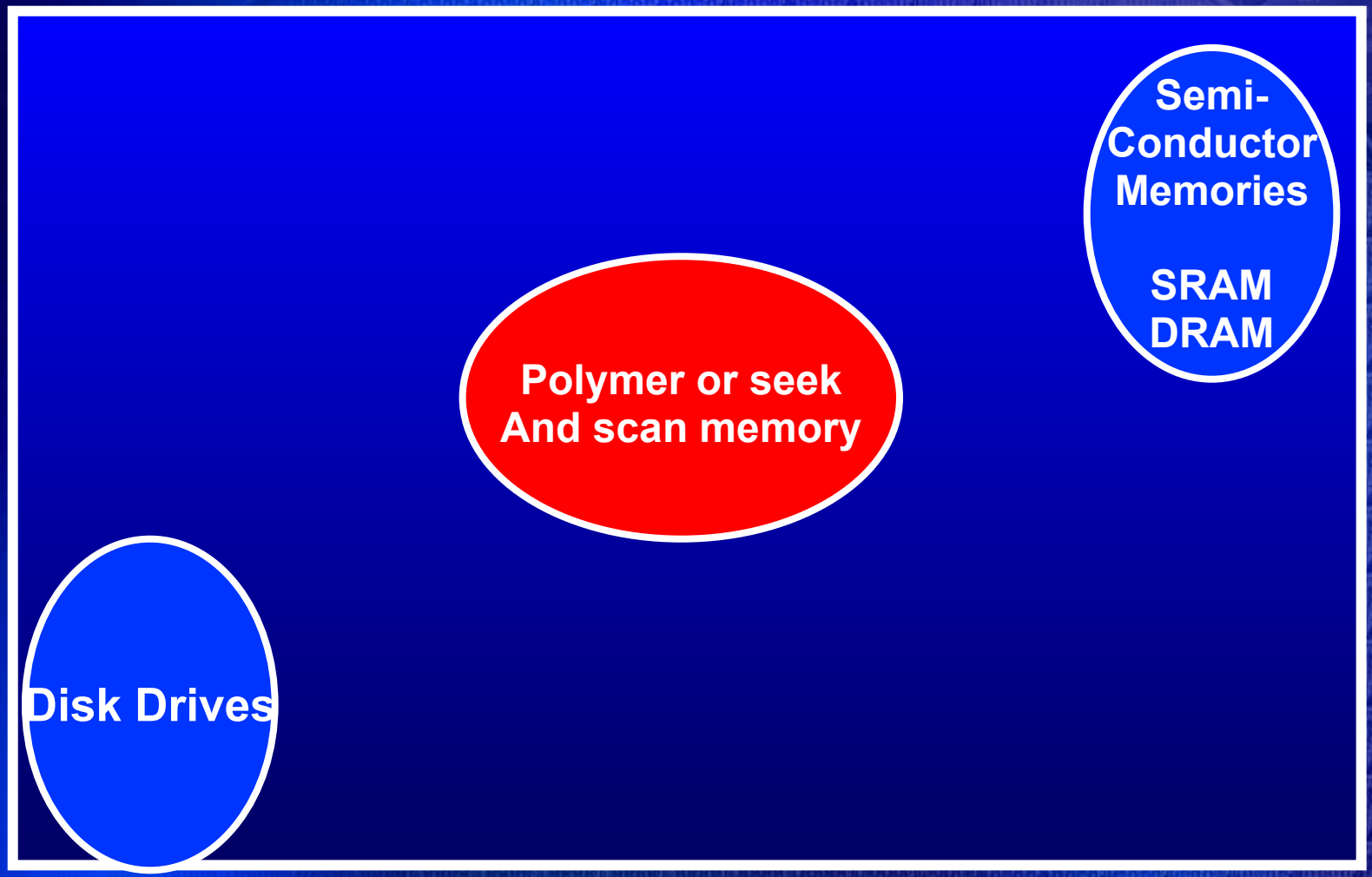
Seek and Scan has best scaling potential

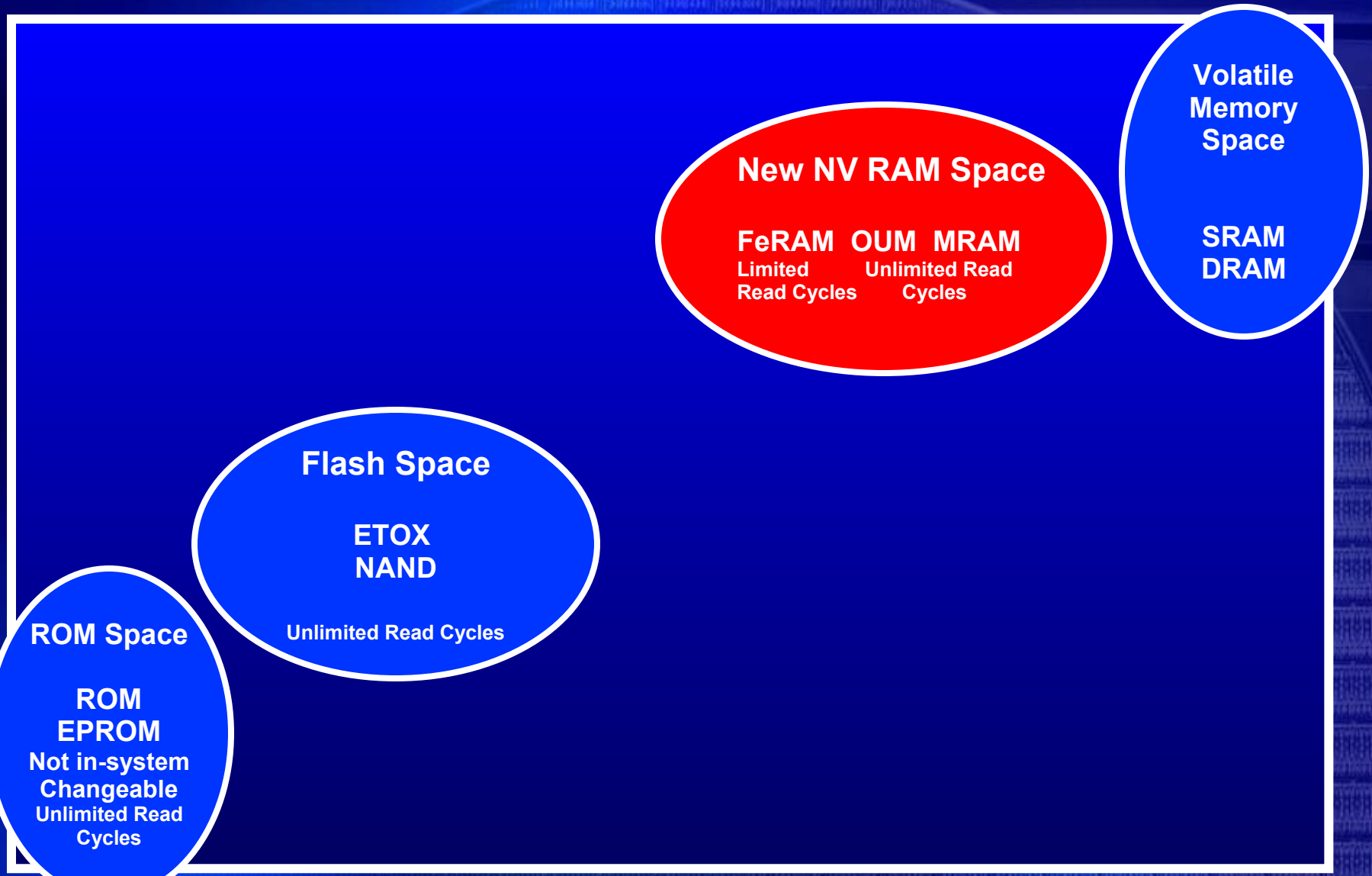


Market Potential

Value of polymer or seek and scan Memory



Value of New NV RAM



Unique Challenges of Non-Volatile Memories

- Commonly accepted NV memory retention time spec is 10 years
- Retention is *NEVER* limited by the typical bits: it is always limited by defect mechanisms
- Storage mechanisms must have high energy barrier for long term stable retention
- In most cases, the write mechanism may cause degradation to either the write mechanism itself or to retention: giving limited cycling capability

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System Consideration

- The new memory technologies are not going to be direct plug and play replacement of conventional memory
- They may operate in different modes and may have higher error rate or higher defect density
- To take best advantage, system architecture should comprehend memory operation
- Error detection and error correction will be an integral part of the future memories

Summary

- Moore's Law will continue through innovation
  - Process complexity will increase to address fundamental limits of physics
- To maintain Moore's Law cost learning curve, difficult to do it by transistor technology alone
  - New opportunity for new memory structures and new materials
- Current mainstream memory technologies of ETOX and NAND will continue to be the key technologies for more than 5 years out

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Summary (continued)

- Many potential new memory technologies
- Simple cross point memory scales better than transistor switch but will always be litho limited
- Multi-layer cross point provides lowest cost opportunities following Moore's Law
- Seek and scan memories can break through the litho barrier and scales more than Moore's Law
- System architecture integral part of memory system